IN THE CLAIMS:

Please amend the claims as follows.

1. (Currently Amended) A fault analysis method for presuming a fault location of a semiconductor IC comprising the steps of:

applying a power supply voltage to said semiconductor IC;

supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC;

storing an analysis point included in said IC, ~~the electric potential~~ a voltage value of which changes by said analysis point in accordance with change of said supplied test pattern, to be corresponding to said test pattern sequence;

measuring a pulse width of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said transient current shows abnormality or not; and

presuming a fault location out of said analysis points based on said test pattern sequence, where the transient power supply current shows abnormality, and said analysis point stored to be corresponding to said test pattern sequence.

2. (Currently Amended) A fault analysis method as claimed in claim 1, wherein said transient power supply current is determined to be abnormal when said pulse width of said transient power supply current is over a predetermined value in said step of determining.

3. (Withdrawn)

4. (Withdrawn)

5. (Currently Amended) A fault analysis method as claimed in ~~any one of~~ claims 2 ~~to 4~~ further comprising a step of:

producing said predetermined value by simulation.

6. (Original) A fault analysis method as claimed in claim 1, wherein said step of presuming a fault location presumes said analysis point, which is placed to be corresponding to all of said test pattern sequence where the transient power supply current shows abnormality, to be said fault location in case said transient power supply current shows abnormality for two or more of said plurality of test pattern sequence.

7. (Original) A fault analysis method as claimed in claim 1, wherein said step of presuming comprises the steps of:

deleting, in case said transient power supply current shows abnormality for two or more test pattern sequence out of said plurality of test pattern sequence, an analysis point, which is not corresponding to the remaining ones of said two or more test pattern sequence, from said analysis points which are corresponding to a predetermined test pattern sequence out of said two or more test pattern sequence; and

presuming a remaining analysis point out of said analysis points corresponding to said predetermined test pattern sequence to be a fault location.

8. (Original) A fault analysis method as claimed in claim 7, wherein said step of deleting includes a step of determining a test pattern sequence, where said transient power supply current shows abnormality first out of said plurality of test

pattern sequence supplied to said semiconductor IC, to be said predetermined test pattern sequence.

9. (Original) A fault analysis method as claimed in claim 1, wherein said step of presuming comprises the steps of:

deleting said analysis points corresponding to the test pattern sequence, where said transient power supply current does not show abnormality, from said analysis points corresponding to the test pattern sequence where said transient power supply current shows abnormality; and

presuming a remaining analysis point out of said analysis points corresponding to said test pattern sequence where said transient power supply current shows abnormality to be a fault location.

10. (Original) A fault analysis method as claimed in claim 1, wherein said step of storing analysis points stores a logic element included in said IC, the output of which changes in accordance with a change of said supplied test pattern, as analysis point to be corresponding to said test pattern sequence.

11. (Currently Amended) A fault analysis method as claimed in claim 1, wherein said step of storing analysis points stores a signal line included in said IC, the ~~electric potential~~ voltage value of which changes in accordance with a change of said supplied test pattern, to be corresponding to said test pattern sequence.

12. (Currently Amended) A fault analysis method as claimed in claim 1, wherein said step of storing analysis points stores a signal transmission path included in said IC to be corresponding to said test pattern sequence, said signal transmission path having: a signal line, the ~~electric potential~~ voltage value of which changes in

accordance with a change of supplied test pattern; and a logic element, the output of which changes in accordance with a change of supplied test pattern, connected to said signal line.

13. (Currently Amended) A fault analysis apparatus for presuming a fault location of a semiconductor IC comprising:

a means for applying a power supply voltage to said semiconductor IC;

a means for supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC;

a means for storing an analysis point included in said IC, the ~~electric potential~~ voltage value of which changes by said analysis point in accordance with change of said supplied test pattern, to be corresponding to said test pattern sequence;

a transient power supply current tester for measuring a pulse width of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said transient current shows abnormality or not; and

a fault location presuming unit for presuming a fault location out of said analysis point based on said test pattern sequence, where the transient power supply current shows abnormality, and said analysis point stored to be corresponding to said test pattern sequence.

14. (Currently Amended) A fault analysis apparatus as claimed in claim 13, wherein said transient power supply current tester determines that said transient power supply current is abnormal when said pulse width of said transient power supply current is over a predetermined value.

15. (Withdrawn)

16. (Withdrawn)

17. (Amended Currently) A fault analysis apparatus as claimed in ~~any one of~~ claims 14 ~~to 16~~, further comprising: a means for producing said predetermined value by simulation.

18. (Original) A fault analysis apparatus as claimed in claim 13, wherein said fault location presuming unit presumes said analysis point, which is placed to be corresponding to all of said test pattern sequence where the transient power supply current shows abnormality, to be said fault location in case said transient power supply current shows abnormality for two or more of said plurality of test pattern sequence.

19. (Original) A fault analysis apparatus as claimed in claim 13, wherein said fault location presuming unit comprises:

a means for deleting, in case said transient power supply current shows abnormality for two or more test pattern sequence out of said plurality of test pattern sequence, an analysis point, which is not corresponding to the remaining ones of said two or more test pattern sequence, from said analysis points which are corresponding to a predetermined test pattern sequence out of said two or more test pattern sequence; and

a means for presuming a remaining analysis point out of said analysis points corresponding to said predetermined test pattern sequence to be a fault location.

20. (Original) A fault analysis apparatus as claimed in claim 19, wherein said means for deleting has a means for determining a test pattern sequence, where said transient power supply current shows abnormality first out of said plurality of test pattern sequence supplied to said semiconductor IC, to be said predetermined test pattern sequence.

21. (Original) A fault analysis apparatus as claimed in claim 13, where in said fault location presuming unit comprises:

a means for deleting said analysis points corresponding to the test pattern sequence, where said transient power supply current does not show abnormality, from said analysis points corresponding to the test pattern sequence where said transient power supply current shows abnormality; and

a means for presuming a remaining analysis point out of said analysis points corresponding to said test pattern sequence where said transient power supply current shows abnormality to be a fault location.

22. (Original) A fault analysis apparatus as claimed in claim 13, wherein said means for storing analysis points stores a logic device, whose output changes in accordance with a change of supplied test pattern, as an analysis point, wherein said logic device is to be corresponding to said test pattern sequence in said semiconductor IC.

23. (Currently Amended) A fault analysis apparatus as claimed in claim 13, wherein said means for storing analysis points stores a signal line included in said IC, the ~~electric potential~~ voltage value of which changes in accordance with a change of

said supplied test pattern, as an analysis point to be corresponding to said test pattern sequence.

24. (Currently Amended) A fault analysis apparatus as claimed in claim 13, wherein said means for storing analysis points stores a signal transmission path included in said IC to be corresponding to said test pattern sequence, said signal transmission path having: a signal line, the ~~electric potential~~ voltage value of which changes in accordance with a change of supplied test pattern; and a logic element, the output of which changes in accordance with a change of supplied test pattern, connected to said signal line.

25. (Currently Amended) A fault analysis apparatus for presuming a fault location of semiconductor IC comprising:

a means for applying a power supply voltage to said semiconductor IC;

a means for supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC;

a means for storing an analysis point included in said IC, the ~~electric potential~~ voltage value of which changes by said analysis point in accordance with change of said supplied test pattern, to be corresponding to said test pattern sequence;

a means for measuring a transient power supply current generated on said semiconductor IC in accordance with a change of said test pattern;

a means for determining that said transient power supply current is abnormal in case pulse width of said transient power supply current is over a predetermined value; and

a means for presuming a fault location out of said analysis point based on said test pattern sequence, where transient power supply current shows abnormality, and said analysis point stored to be corresponding to said test pattern sequence.

26. (Withdrawn)

27. (Withdrawn)